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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/655,385	GANTON	
	Examiner	Art Unit	
	Corey P. Chau	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-24 and 26-28* is/are rejected.

7)☒ Claim(s) *25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 1-28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

2. Claim 1 has been amended to recite "removing the test voltage to the device audio interface port; and, supplying an audio signal to the device audio interface port after removing the test voltage", which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 2-9 are rejected for depending on a rejected claim. Claims 10 and 28 are rejected for the same reason stated above for claim 1. Claims 11-27 are rejected for depending on a rejected claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application

by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-2, 5-10, 13, 16-20, 23-24, and 26-28 are rejected under 35 U.S.C. 102(b) as being anticipated by USPN 5978689 to Tuoriniemi et al. (hereafter as Tuoriniemi).

5. Regarding Claim 1, as best understood with regards to the 112, 1st problem mention above, Tuoriniemi discloses in an electrical device having an audio interface port, a method for identifying a headset plugged into the device audio interface port (Figs. 2-3, 6, and 8), the method comprising:

supplying a test voltage to a device audio interface port (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 4, line 59 to column 5, line 29);

measuring a voltage level at the device audio interface port (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 5, lines 9-29; column 8, lines 21-53; column 9, lines 1-32);

identifying a headset type plugged into the device audio interface port in response to measuring the voltage level (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 5, lines 9-29; column 8, lines 21-53; column 9, lines 1-32);

removing the test voltage to the device audio interface port (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 4, line 59 to column 5, line 29); and,

supplying an audio signal to the device audio interface port after removing the test voltage (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 4, line 59 to column 5, line 29).

6. Regarding Claim 2, Tuoriniemi discloses measuring a voltage level at the device audio interface port includes comparing the measured voltage level to a threshold value; and, wherein identifying a headset type in response to measuring the voltage level includes identifying a headset type in response to comparing the measured voltage level to a threshold value (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 5, lines 9-29; column 8, lines 21-53; column 9, lines 1-32).

7. Regarding Claim 5, Tuoriniemi discloses measuring a voltage level at the device audio interface port includes: driving a network with the test voltage and dividing the test voltage between a resistance for the network and a resistance for the headset; and, measuring a divided test voltage at the audio interface port (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 5, lines 9-29; column 8, lines 21-53; column 9, lines 1-32).

8. Regarding Claim 6, Tuoriniemi discloses measuring the divided test voltage at the audio interface port includes: accepting an analog voltage; converting the analog voltage to a digital signal; and, interpreting the digital signal (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 5, lines 9-59; column 8, lines 21-53; column 9, lines 1-32).

9. Regarding Claim 7, Tuoriniemi discloses wherein the supplying the audio signal to the device audio interface port comprises supplying a stereo audio signal in response to identifying a stereo headset (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 5, lines 9-29; column 8, lines 21-53; column 9, lines 1-32).

10. Regarding Claim 8, Tuoriniemi discloses driving a network with the test voltage and dividing the test voltage between a resistance for the network and a resistance for the headset includes using the network to reduce a rate of change for the voltage at the device audio interface port (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 5, lines 9-29; column 8, lines 21-53; column 9, lines 1-32).

11. Regarding Claim 9, Tuoriniemi discloses plugging the headset into the device audio interface port; and, detecting, in the device, the presence of the headset (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 5, lines 9-29; column 8, lines 21-53; column 9, lines 1-32).

12. Regarding Claim 10, as best understood with regards to the 112, 1st problem mention above, Tuoriniemi discloses in an electrical device having an audio interface port, a system for identifying a headset plugged into the device audio interface port, the system comprising:

an audio interface port to accept variable impedance headphone jacks (Figs. 2-3, 6, and 8-10);

a first switch with an input connected to receive a test voltage, a control input to accept a switch control signal, and an output to supply the test voltage in response to the switch control signal, the test voltage being removed when audio signals are

supplied to the audio interface; (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 5, lines 9-29);

a test network with a first port connected to the first switch output and a second port connected to the audio interface port, the test network to condition current to the audio interface port (Figs. 2-3, 6; and 8-10; column 4, lines 35-46; column 5, lines 9-29; column 8, lines 21-53; column 9, lines 1-32); and,

an identification sub-system with an input connected to the audio interface port and an output to supply the switch control signal, the identification sub-system determining voltage levels at the audio interface port and comparing voltage levels with a first predetermined threshold value to identify a headset type connected to the audio interface port (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 5, lines 9-29; column 8, lines 21-53; column 9, lines 1-32).

13. Regarding Claim 13, Tuoriniemi discloses a test voltage source with an output connected to the first switch input; and, wherein the identification sub-system includes: a voltage determination sub-system with an input connected to the audio interface port and an output to supply a determination signal responsive to the voltage at the audio interface port; and, a controller having an input connected to the voltage determination sub-system output and an output to supply the switch control signal, the controller comparing determination signals with a second predetermined threshold value to identify a headset type connected to the audio interface port (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 5, lines 9-29; column 8, lines 21-53; column 9, lines 1-32).

14. Regarding Claim 16, Tuoriniemi discloses a microcontroller logic unit with an input and a first output connected to the test network first port; and, wherein the controller, the test voltage source, and the first switch are included in the microcontroller logic unit, the controller input and the voltage determination sub-system output are connected to the logic unit input, and the first switch output is connected to the logic unit first output (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 5, lines 9-29; column 8, lines 21-53; column 9, lines 1-32).

15. Regarding Claim 17, Tuoriniemi discloses the voltage determination sub-system is an analog-to-digital converter (ADC) with an input connected to the audio interface port and an output connected to the logic unit input (Figs. 2-3, 6, and 8-10; column 4, lines 35-46; column 5, lines 9-59; column 8, lines 21-53; column 9, lines 1-32).

16. Regarding Claim 18, Tuoriniemi discloses the test network includes a first resistor with a first end connected to the logic unit first output and a second end connected to the audio interface port (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 29; column 8, lines 21-53; column 9, lines 1-32).

17. Regarding Claim 19, Tuoriniemi discloses the test network further includes a first capacitor with a first end connected to the first resistor second end and a second end connected to ground (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 29; column 8, lines 21-53; column 9, lines 1-32).

18. Regarding Claim 20, Tuoriniemi discloses the test network further includes a second switch with a first port connected to the first capacitor second end, a second port connected to ground, and a control input to accept first control signals, the second

switch to close in response to accepting a first test control signal; and, wherein the logic unit includes a second output to supply first control signals, the output to supply the first test control signal in response to the logic unit supplying a test voltage at the first output (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 6, line 8; column 8, lines 21-53; column 9, lines 1-32).

19. Regarding Claim 23, Tuoriniemi discloses the test network further includes a second resistor with a first end connected to the first resistor second end and a second end connected to the audio interface port (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 29; column 8, lines 21-53; column 9, lines 1-32).

20. Regarding Claim 24, Tuoriniemi discloses a digital-to-analog converter (DAC) with an input to accept a stereo control signal and an output connected to the audio interface port, the output to supply stereo signals in response to accepting the stereo control signal; and, wherein the logic unit includes a third output connected to the DAC input, the third output to supply the stereo control signal in response to the logic unit identifying a stereo headset on the audio interface port (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 29; column 8, lines 21-53; column 9, lines 1-32).

21. Regarding Claim 26, as best understood with regards to the 112, 1st problem mention above, Tuoriniemi discloses a blocking network with a first port connected to the DAC output and a second port connected to the audio interface port (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 29; column 8, lines 21-53; column 9, lines 1-32).

22. Regarding Claim 27, Tuoriniemi discloses the audio interface port with at least four lines; and, the headset plugged into the audio interface port (Figs. 2-3, 6, and 8-10).

23. Regarding Claim 28, Tuoriniemi discloses in an electrical device having an audio interface port, a system for identifying a headset plugged into the device audio interface port, the system comprising:

the audio interface port (Figs. 2-3, 6, and 8-10);

a headset plugged into the audio interface port (Figs. 2-3, 6, and 8-10);

an analog-to-digital converter (ADC) with an input connected to the audio interface port and an output to supply a determination signal responsive to a voltage level on the audio interface port (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 59; column 8, lines 21-53; column 9, lines 1-32);

a microcontroller logic unit with: a first output to supply a test voltage signal, the test voltage being removed when audio signals are supplied to the audio interface port (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 59; column 8, lines 21-53; column 9, lines 1-32);

an input to accept the determination signal, the logic unit to compare determination signal values with a predetermined threshold value to identify a headset type connected to the audio interface port (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 29; column 8, lines 21-53; column 9, lines 1-32); and

a second output to supply a stereo control signal in response to identifying a stereo headset (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 29; column 8, lines 21-53; column 9, lines 1-32);

a test network including:

a first resistor with a first end connected to the logic unit first output and a second end (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 29; column 8, lines 21-53; column 9, lines 1-32);

a capacitor with a first end connected to the first resistor second end and a second end connected to ground (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 29; column 8, lines 21-53; column 9, lines 1-32); and,

a second resistor with a first end connected to the first resistor second end and a second end connected to the audio interface port (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 29; column 8, lines 21-53; column 9, lines 1-32);

a digital-to-analog converter (DAC) with an input connected to the logic unit second output and an output to supply stereo audio signals in response to the DAC accepting a stereo control signal (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 6, line 8; column 8, lines 21-53; column 9, lines 1-32); and, a blocking network including:

a capacitor with a first end connected to the DAC output and a second end (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 29; column 8, lines 21-53; column 9, lines 1-32); and,

a resistor with a first end connected to the capacitor second end and a second end connected to the audio interface port (Figs. 2-3, 6, and 8-10; column 4, line 35 to column 5, line 29; column 8, lines 21-53; column 9, lines 1-32).

24. Claims 1-24 and 26-28 are rejected under 35 U.S.C. 102(e) as being anticipated by USPN 6594366 to Adams.

25. Regarding Claim 1, as best understood with regards to the 112, 1st problem mention above, Adams discloses in an electrical device having an audio interface port, a method for identifying a headset plugged into the device audio interface port (Figs. 2-4), the method comprising:

supplying a test voltage to a device audio interface port (Figs. 2-4; column 2, lines 19-47; column 3, lines 5-33; column 4, line 26-45);

measuring a voltage level at the device audio interface port (Figs. 2-4; column 2, lines 19-47; column 3, line 5 to column 4, line 44);

identifying a headset type plugged into the device audio interface port in response to measuring the voltage level (Figs. 2-4; column 2, lines 19-47; column 3, line 5 to column 4, line 44);

removing the test voltage to the device audio interface port (Figs. 2-4; column 2, lines 19-47; column 3, lines 5-33; column 4, line 26-45); and,

supplying an audio signal to the device audio interface port after removing the test voltage (Figs. 2-4; column 2, lines 19-47; column 3, lines 5-33; column 4, line 26-45).

26. Regarding Claim 2, Adams discloses measuring a voltage level at the device audio interface port includes comparing the measured voltage level to a threshold value; and, wherein identifying a headset type in response to measuring the voltage level includes identifying a headset type in response to comparing the measured voltage level to a threshold value (Figs. 2-4; column 2, lines 19-47; column 3, line 5 to column 4, line 44).

27. Regarding Claim 3, Adams discloses identifying a headset type in response to comparing the measured voltage level to a threshold value includes: identifying a stereo headset for a measured voltage level greater than the threshold value; and, identifying a mono headset for a measured voltage level less than the threshold value (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

28. Regarding Claim 4, Adams discloses identifying a headset type in response to comparing the measured voltage level to a threshold value includes: identifying a stereo headset for a measured voltage level less than the threshold value; and, identifying a mono headset for a measured voltage level greater than the threshold value (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

29. Regarding Claim 5, Adams discloses measuring a voltage level at the device audio interface port includes: driving a network with the test voltage and dividing the test voltage between a resistance for the network and a resistance for the headset; and, measuring a divided test voltage at the audio interface port (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

30. Regarding Claim 6, Adams discloses measuring the divided test voltage at the audio interface port includes: accepting an analog voltage; converting the analog voltage to a digital signal; and, interpreting the digital signal (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

31. Regarding Claim 7, Adams discloses wherein the supplying the audio signal to the device audio interface port comprises supplying a stereo audio signal in response to identifying a stereo headset (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

32. Regarding Claim 8, Adams discloses driving a network with the test voltage and dividing the test voltage between a resistance for the network and a resistance for the headset includes using the network to reduce a rate of change for the voltage at the device audio interface port (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

33. Regarding Claim 9, Adams discloses plugging the headset into the device audio interface port; and, detecting, in the device, the presence of the headset (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

34. Regarding Claim 10, as best understood with regards to the 112, 1st problem mention above, Adams discloses in an electrical device having an audio interface port, a system for identifying a headset plugged into the device audio interface port, the system comprising:

an audio interface port to accept variable impedance headphone jacks (Figs. 2-4);

a first switch with an input connected to receive a test voltage, a control input to accept a switch control signal, and an output to supply the test voltage in response to the switch control signal, the test voltage being removed when audio signals are supplied to the audio interface (Figs. 2-4; column 2, lines 19-47; column 3, lines 5-33);

a test network with a first port connected to the first switch output and a second port connected to the audio interface port, the test network to condition current to the audio interface port (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44); and,

an identification sub-system with an input connected to the audio interface port and an output to supply the switch control signal, the identification sub-system determining voltage levels at the audio interface port and comparing voltage levels with a first predetermined threshold value to identify a headset type connected to the audio interface port (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

35. Regarding Claim 11, Adams discloses the identification sub-system identifies a stereo headset in response to determining a voltage level above the first threshold value and a mono headset in response to determining a voltage level below the first threshold value (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

36. Regarding Claim 12, Adams discloses the identification sub-system identifies a stereo headset in response to determining a voltage level below the first threshold value and a mono headset in response to determining a voltage level above the first threshold value (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

37. Regarding Claim 13, Adams discloses a test voltage source with an output connected to the first switch input; and, wherein the identification sub-system includes: a voltage determination sub-system with an input connected to the audio interface port and an output to supply a determination signal responsive to the voltage at the audio interface port; and, a controller having an input connected to the voltage determination sub-system output and an output to supply the switch control signal, the controller comparing determination signals with a second predetermined threshold value to identify a headset type connected to the audio interface port (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

38. Regarding Claim 14, Adams discloses the controller identifies a stereo headset connected to the audio interface port in response to accepting a determination signal with a value above the second predetermined threshold value and a mono headset in response to accepting a determination signal with a value below the second threshold value (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

39. Regarding Claim 15, Adams discloses the controller identifies a stereo headset connected to the audio interface port in response to accepting a determination signal with a value below the second predetermined threshold value and a mono headset in response to accepting a determination signal with a value above the second threshold value (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

40. Regarding Claim 16, Adams discloses a microcontroller logic unit with an input and a first output connected to the test network first port; and, wherein the controller, the test voltage source, and the first switch are included in the microcontroller logic unit, the

controller input and the voltage determination sub-system output are connected to the logic unit input, and the first switch output is connected to the logic unit first output (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

41. Regarding Claim 17, Adams discloses the voltage determination sub-system is an analog-to-digital converter (ADC) with an input connected to the audio interface port and an output connected to the logic unit input (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

42. Regarding Claim 18, Adams discloses the test network includes a first resistor with a first end connected to the logic unit first output and a second end connected to the audio interface port (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

43. Regarding Claim 19, Adams discloses the test network further includes a first capacitor with a first end connected to the first resistor second end and a second end connected to ground (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

44. Regarding Claim 20, Adams discloses the test network further includes a second switch with a first port connected to the first capacitor second end, a second port connected to ground, and a control input to accept first control signals, the second switch to close in response to accepting a first test control signal; and, wherein the logic unit includes a second output to supply first control signals, the output to supply the first test control signal in response to the logic unit supplying a test voltage at the first output (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

45. Regarding Claim 21, Adams discloses the second switch is a transistor with a first terminal connected to the first capacitor second end, a second terminal connected to ground, and a control terminal connected to the logic unit second output, the transistor being enabled in response to accepting the first test control signal (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

46. Regarding Claim 22, Adams discloses the transistor is selected from the group including field effect transistors (FETs) and bi-polar junction transistors (BJTs) (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

47. Regarding Claim 23, Adams discloses the test network further includes a second resistor with a first end connected to the first resistor second end and a second end connected to the audio interface port (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

48. Regarding Claim 24, Adams discloses a digital-to-analog converter (DAC) with an input to accept a stereo control signal and an output connected to the audio interface port, the output to supply stereo signals in response to accepting the stereo control signal; and, wherein the logic unit includes a third output connected to the DAC input, the third output to supply the stereo control signal in response to the logic unit identifying a stereo headset on the audio interface port (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

49. Regarding Claim 26, Adams discloses a blocking network with a first port connected to the DAC output and a second port connected to the audio interface port (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

50. Regarding Claim 27, Adams discloses the audio interface port with at least four lines; and, the headset plugged into the audio interface port (Figs. 2-4).

51. Regarding Claim 28, as best understood with regards to the 112, 1st problem mention above, Adams discloses in an electrical device having an audio interface port, a system for identifying a headset plugged into the device audio interface port, the system comprising:

the audio interface port (Figs. 2-4);

a headset plugged into the audio interface port (Figs. 2-4);

an analog-to-digital converter (ADC) with an input connected to the audio interface port and an output to supply a determination signal responsive to a voltage level on the audio interface port;

a microcontroller logic unit with: a first output to supply a test voltage signal, the test voltage being removed when audio signals are supplied to the audio interface port (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44);

an input to accept the determination signal, the logic unit to compare determination signal values with a predetermined threshold value to identify a headset type connected to the audio interface port (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44); and

a second output to supply a stereo control signal in response to identifying a stereo headset (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44);

a test network including:

a first resistor with a first end connected to the logic unit first output and a second end (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44);

a capacitor with a first end connected to the first resistor second end and a second end connected to ground (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44); and,

a second resistor with a first end connected to the first resistor second end and a second end connected to the audio interface port (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44);

a digital-to-analog converter (DAC) with an input connected to the logic unit second output and an output to supply stereo audio signals in response to the DAC accepting a stereo control signal (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44); and, a blocking network including:

a capacitor with a first end connected to the DAC output and a second end (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44); and,

a resistor with a first end connected to the capacitor second end and a second end connected to the audio interface port (Figs. 2-4; column 2, lines 19-65; column 3, line 5 to column 4, line 44).

Allowable Subject Matter

52. Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

53. Applicant's arguments filed 3/15/2007 have been fully considered but they are not persuasive.

54. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the test voltage is a discrete voltage) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

55. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection (i.e. 112, 1st).

Conclusion

56. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

57. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey P. Chau whose telephone number is 571-272-7514. The examiner can normally be reached on Monday-Friday, 9:00am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on 571-272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VIVIAN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600
5/29/07

May 29, 2007
CPC